Two-Channel Atom Chip Driver
User’s Manual

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1. Safety Notices

1.1 WARNINGS

The following warning and cautions are applicable to this device:

**GROUNDS** - The atom chip driver must be connected to AC (mains) power using a three-wire power cord with a protective ground contact. Always use a three-prong outlet that is properly grounded. Do not operate the device with any two-conductor outlet or extension cord. If using an extension cord, use a three-conductor version.

**LINE FUSE** - Only use line fuses with the required rated current and voltage, and the specified type (normal blow, time delay, etc.). Do not use repaired fuses or short-circuited fuse holders; to do so could cause a shock or fire hazard.

**INTERNAL ADJUSTMENTS** - Internal adjustments should be made only by trained service personnel. When performing internal adjustments, use adequate safety precautions to prevent the risk of electric shock. *High voltages from the AC (mains) power line will be present!*

**LINE VOLTAGE SELECTION** – The atom chip driver can operate from an AC (mains) power source with voltage between 90 and 264 VAC and a line frequency between 47 and 63 Hz. There is no line voltage selection switch - the chip driver’s power supply will automatically adjust its operation for the applied line voltage.
The following symbols are used in this manual:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Caution Symbol" /></td>
<td>Caution! – Risk of electric shock</td>
</tr>
<tr>
<td><img src="image" alt="Caution Symbol" /></td>
<td>Caution! – Risk of damage to equipment</td>
</tr>
<tr>
<td><img src="image" alt="Earth Symbol" /></td>
<td>Earth ground</td>
</tr>
<tr>
<td><img src="image" alt="Reference Symbol" /></td>
<td>Reference Ground (not necessarily connected to earth ground)</td>
</tr>
<tr>
<td><img src="image" alt="Voltage Source Symbol" /></td>
<td>Voltage Source</td>
</tr>
<tr>
<td><img src="image" alt="Amplifiers Symbol" /></td>
<td>Amplifiers (op-amp, line driver, receiver, etc.)</td>
</tr>
<tr>
<td><img src="image" alt="Resistor Symbol" /></td>
<td>Resistor or General Impedance</td>
</tr>
<tr>
<td><img src="image" alt="Capacitor Symbol" /></td>
<td>Capacitor</td>
</tr>
<tr>
<td><img src="image" alt="Twisted-Pair Cable Symbol" /></td>
<td>Twisted-Pair Cable</td>
</tr>
</tbody>
</table>
1.3 PACKAGE CONTENTS

Upon receiving the atom chip driver, inspect the packaging for damage. If the packaging shows signs of damage or excessive shock, notify the shipping company and then contact ColdQuanta. Keep packing materials, per the instructions of the shipping company.

The shipment should contain the following items:

- Atom chip driver
- Input cables with attached three-pin LEMO plugs, quantity = 2
- Output cables with attached two-pin LEMO plugs, quantity = 2
- Three-prong power cord
- User’s manual (this document)

If any of these items are missing, please contact ColdQuanta to obtain replacements.
## 2. Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Current(^1)</td>
<td>(I_0)</td>
<td>0 &lt; (R_{LOAD}) &lt; 0.5 (\Omega)</td>
<td>-5</td>
<td>+5</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5 &lt; (R_{LOAD}) &lt; 1 (\Omega)</td>
<td>-3</td>
<td>+3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Voltage Input Range</td>
<td></td>
<td></td>
<td>-5</td>
<td>+5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Differential</td>
<td>(V_i)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Common-Mode</td>
<td>(V_{CM})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Impedance</td>
<td></td>
<td>DC Resistance</td>
<td>9.99</td>
<td>20</td>
<td>10.1</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>Differential</td>
<td>(Z_i)</td>
<td>DC Resistance</td>
<td></td>
<td></td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td>Common-Mode</td>
<td>(Z_{CM1}, Z_{CM2})</td>
<td>DC Resistance</td>
<td></td>
<td></td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td>Accuracy</td>
<td></td>
<td>(V_i = 0)</td>
<td>-50</td>
<td>0.1</td>
<td>50</td>
<td>%</td>
</tr>
<tr>
<td>Zero-Point Offset</td>
<td></td>
<td></td>
<td>0.999</td>
<td></td>
<td>60</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Slope</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(V/A)</td>
</tr>
<tr>
<td>Current Monitor</td>
<td></td>
<td></td>
<td>0.99</td>
<td>1.00</td>
<td>1.01</td>
<td>V/(A)</td>
</tr>
<tr>
<td>Slope</td>
<td></td>
<td></td>
<td></td>
<td>31</td>
<td></td>
<td>(kHz)</td>
</tr>
<tr>
<td>Bandwidth(^2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(kHz)</td>
</tr>
<tr>
<td>eFuse(^3)</td>
<td></td>
<td></td>
<td>0.1</td>
<td>10.1</td>
<td></td>
<td>s</td>
</tr>
<tr>
<td>Charge Time Constant</td>
<td>(\tau_c)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>s</td>
</tr>
<tr>
<td>Decay Time Constant</td>
<td>(\tau_d)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>s</td>
</tr>
<tr>
<td>Trip Voltage</td>
<td></td>
<td></td>
<td>Set internally</td>
<td>1.00</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Dynamic Performance(^4)</td>
<td></td>
<td>(R_{LOAD} = 0.5 (\Omega))</td>
<td>47</td>
<td>5</td>
<td>95</td>
<td>(kHz)</td>
</tr>
<tr>
<td>Full Power Bandwidth (-3 dB)</td>
<td></td>
<td>(\pm 5 \rightarrow 5 (A); R_{LOAD} = 0.5 (\Omega))</td>
<td></td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Step Response(^5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(kHz)</td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)</td>
<td></td>
<td>(R_{LOAD} = 0.1 (\Omega))</td>
<td>0.04%</td>
<td>0.4%</td>
<td>1.0%</td>
<td>%</td>
</tr>
<tr>
<td>f = 1 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>f = 5 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>f = 10 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>f = 30 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio (CMRR)</td>
<td></td>
<td>(Z_0 = 100 (\Omega))</td>
<td>96</td>
<td>95</td>
<td>82</td>
<td>dB</td>
</tr>
<tr>
<td>f = 100 Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>f = 1 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>f = 10 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>f = 100 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>AC Power Requirements</td>
<td>Voltage</td>
<td></td>
<td>110</td>
<td>240</td>
<td></td>
<td>(VAC)</td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
<td></td>
<td>47</td>
<td>63</td>
<td></td>
<td>(Hz)</td>
</tr>
<tr>
<td>Physical</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dimensions</td>
<td>(h \times w \times d)</td>
<td>3.47 × 8.37 × 16</td>
<td>10</td>
<td>4.54</td>
<td></td>
<td>inches</td>
</tr>
<tr>
<td>Weight</td>
<td>(h \times w \times d)</td>
<td>8.7 × 21.3 × 40.6</td>
<td></td>
<td></td>
<td></td>
<td>lbs</td>
</tr>
</tbody>
</table>

\(^1\) Output currents are only specified for load resistances \(R_{LOAD} < 1 \(\Omega\)\). The ranges of \(R_{LOAD}\) listed do not account for the resistance of the output cable. For the 6' RG58 output cables supplied with the unit, the maximum current that can be driven through a load \(R_{LOAD} = 0.5 \(\Omega\)\) is \(\pm 4.8 \(A\)\).

\(^2\) The current monitor bandwidth is only specified when connected to a high-impedance load, such as an oscilloscope input.

\(^3\) The charge and decay time constants cannot be independently set simultaneously. See Section 7 for more information about the relationship between these values, and how to set them.

\(^4\) The bandwidth depends on the inductance and capacitance of the output cable. The specified value of 47 \(kHz\) corresponds to a 6' length of RG-58 cable. See Section 6 for more details.

\(^5\) Values from 10% to 90% of the pulse height.
3. Typical Performance

Figure 1: Current Noise Spectrum (Negative Output)

Figure 2: Current Noise Spectrum (Positive Output)

Figure 3: Crosstalk
4. Description

4.1 Overview

ColdQuanta’s atom chip driver consists of two bidirectional voltage-controlled current sources that are designed to drive two atom chip traces. The output currents are directly proportional to the input voltage, i.e. an input voltage of +1.0 V will set the output current to +1.0 A. Each channel is independently capable of driving up to ±5 A. The two channels are floating, and each has its own set of controls, indicators, inputs, and outputs. Balanced, differential inputs isolate the chip driver from control electronics. To accommodate atom chip traces that overlap, the two outputs are isolated from each other and from ground.

Figures 4 and 5 show the layouts of the front and rear panels, respectively. Descriptions of the switches, jacks, and indicators appear throughout this section.

4.2 Power Requirements

The chip driver is powered with a standard three-prong power cord that inserts into the AC Power Module on the rear panel (see Figure 5). The unit can operate from a 110 to 240 V AC (mains) power source with a line frequency of 47 to 63 Hz. The AC power module contains the line fuse, which is a medium-blow type rated at 1 A / 250 V and measuring 5 × 20 mm.

**HIGH VOLTAGE WARNING!**

The atom chip driver must be connected to AC (mains) power using a three-wire power cord with a protective ground contact. Always use a three-prong outlet that is properly grounded. Do not operate the device with any two-conductor outlet or extension cord. If using an extension cord, use a three-conductor version.

**HIGH VOLTAGE WARNING!**

Only use line fuses with the required rated current and voltage, and the specified type (normal blow, time delay, etc.). Do not use repaired fuses or short-circuited fuse holders; to do so could cause a shock or fire hazard.
4.3 **OPERATION**

To turn on to the chip driver, use the “Main Power” switch on the far left side of the front panel. Applying power to the chip driver does not turn on the output current to the atom chip.

The two black buttons on the front panel marked “Output On/Off” are used to enable and disable the output current of each channel. By pressing this button, an internal relay electrically connects that channel’s output to the load; pressing this button again unlatches the relay, breaking the electrical connection to the load. When a channel is enabled, the blue LED on the “Output On/Off” button will be illuminated.

When a channel’s output is enabled, a fault condition will automatically disable that output. The output can be re-enabled by pressing the “Output On/Off” button again. Pressing this button resets all faults conditions; however, if the fault condition still exists, the output will be immediately disabled.

4.4 **MONITORS**

Each channel has two monitor BNC outputs:

- **Current Monitor** – The voltage on this output is equal to the output current.
- **eFuse Monitor** – The voltage on this output indicates how close the eFuse circuit is to tripping. At 1 V, the eFuse circuit will trip. More details on this protection circuit appear in Section 7 below.

The outputs of both monitors are referenced to earth ground.
Figure 4: Front panel layout of the two-channel atom chip driver.

Figure 5: Rear panel layout of the two-channel atom chip driver.
4.5 FAULTS

Several protection features have been incorporated into the atom chip driver to protect both the atom chip and the driver itself. Fault conditions are indicated with the LEDs on the front panel. These faults are:

- **eFuse Open** – When a large current has been applied to the load for a long enough duration, the eFuse circuit will trip. When this fault occurs, the “eFuse Open” LED will illuminate and the output will be disabled. See Section 7 for more information about the eFuse circuit.

- **Overtemp** – The chip driver is designed to operate continuously with both channels outputting currents up to ±5 A. However, blocking the air intake on the rear panel (see Figure 5) may cause the internal temperature to exceed the high temperature limit. If this happens, the “Overtemp” LED will illuminate and the output will be disabled.

- **Open Circuit** – If no load is connected to the output, the “Open Circuit” LED will illuminate when the user tries to enable the output. If this happens, check the cable from the chip driver to the atom chip for bad connections.
5. Input Controls

The current outputs of the chip driver are controlled with input voltages applied to the LEMO jacks at the top-left corner of the rear panel (see Figure 5). The output current, in amperes, is equal to the differential input voltage, in volts. Clamping diodes on the input prevent the voltage on each input from exceeding ±12 V (with respect to the chip driver’s internal ground).

To reject ground noise and electromagnetic interference, and to ensure that the two channels remain floating, the inputs are configured as balanced receivers with very high common-mode input impedances. This architecture is particularly useful for rejecting pick-up at 50/60 Hz and its harmonics, as current noise at these frequencies can “shake” the atom trap, causing the atoms to slosh and heat up.

The subject of balanced circuitry and common-mode rejection is too extensive to be thoroughly reviewed here. For readers who want to learn more about this topic, several references are provided [1-5]. In particular, this subject arises extensively in high-end and professional audio, and many useful discussions can be found within this community.

5.1 Pin Connections

Figure 6 shows the pin diagram for the input LEMO connectors. The chip driver will output a positive current when the voltage applied to the + terminal (pin 2) is larger than the voltage applied to the – terminal (pin 3). Pin 1, which is closest to the red notch, is unconnected inside of the chip driver.

![Pin Diagram](image)
The + and – inputs together form a balanced receiver. Here, the chip driver’s output, in amperes, is equal to the voltage difference, in volts, applied across the two inputs. The DC resistance from each of these inputs to the chip driver’s internal ground is 10 MΩ.

The use of balanced inputs serves two important functions. First, very high impedances ensure that the two chip driver channels remain well-isolated (i.e. floating) from each other when driving crossing chip wires. Second, balanced inputs provide excellent common-mode rejection, helping to keep the inputs less susceptible to electromagnetic interference and ground noise.

To better understand how balanced circuitry provides common-mode rejection, Figure 7 shows a schematic of a voltage source connected to one of the chip driver’s inputs. Here, a line driver outputs a differential signal onto two lines labeled HI and LO. These lines have (common-mode) source impedances $Z_{01}$ and $Z_{02}$, and a differential source impedance of $Z_{01} + Z_{02}$. At the chip driver, the (common-mode) load impedances to the chip driver’s ground are $Z_{CM1}$ and $Z_{CM2}$, and the differential load impedance is $Z_I$.

In the atom chip driver, the receiver is a differential amplifier that produces an output only in response to a potential difference across its inputs. As a result, common-mode signals (i.e. signals that appear identically on both of the inputs) are suppressed via subtraction. Assume that the driver is referenced to a ground that has superimposed on it a noise voltage, as measured with respect to the receiver’s ground. The voltage at each of the receiver’s inputs, again measured with respect to the receiver’s ground, is the sum of the desired transmitted signal and the unwanted ground noise voltage. The ground noise will appear identically on both of the inputs, and therefore will be removed by the receiver upon subtraction.

Figure 7: The atom chip driver uses a balanced receiver to reject ground noise, provide immunity to electromagnetic interference, and ensure floating outputs.
5.3 Balanced Line Drivers

The chip driver’s inputs must be properly driven to maximize common-mode rejection. To see this, note that the voltage on the HI line will be slightly reduced due to the voltage divider formed by $Z_{01}$ and $Z_{CM1}$. Similarly, the voltage on the LO line will also be reduced, this time by the voltage divider formed by $Z_{02}$ and $Z_{CM2}$. For perfect subtraction of common-mode signals, the voltage dividers should be matched as well as possible. Given the limitations imposed by the 1% tolerance of typical resistors, the mismatch between the two voltage dividers can be minimized by reducing the source impedances and increasing the load impedances, i.e. $Z_0 \ll Z_{CM}$.

To meet this condition for $Z_{CM} = 10 \, \text{M}\Omega$, the driver should have a low output impedance. For example, with $Z_0 = 100 \, \Omega$ the voltage on each line will be reduced by a factor of $10 \, \text{M}\Omega / (100 \, \Omega + 10 \, \text{M}\Omega) \approx 0.99999$. Assuming that the source impedances are set with resistors with a tolerance of 1%, the voltage dividers on the HI and LO lines will be matched to 1 part in $10^{-7}$, corresponding to a common-mode rejection ratio (CMRR) of $20 \log 10^{-7} = -140 \, \text{dB}$. The actual CMRR that can be attained will be limited by the performance of the receiver’s subtraction circuit. Actual CMRR values typically exceed 90 dB for frequencies up to 1 kHz.

Figure 8 shows three op-amp circuits recommended as balanced line drivers. Figure 8a shows the simplest line driver: a single op-amp buffer. Here, the source impedances for the HI and LO lines are set by R2 and R3, respectively. The line impedances are balanced when $R2 = R3$.

The circuit in Figure 8a assumes a perfect op-amp, i.e. one with zero output impedance. While this is a good assumption at low frequencies, real-world op-amps have output impedances that increase with frequency (usually a result of stray inductance in the op-amp leads). Due to this frequency-dependence, the source impedances of the two lines can become unbalanced at higher frequencies. The circuit in Figure 8b is a solution: buffer the driver GND with the same op-amp used to buffer the INPUT signal. For convenience, the two buffers can be part of a dual op-amp packaged in a single chip. Now, the frequency dependence of the two source impedances will be matched, helping to prevent degradation of CMRR at higher frequencies.
Figure 8c shows a circuit that may offer additional noise rejection when used with certain digital-to-analog converters (DACs). Here, both the + and – inputs of the chip driver are driven with voltages produced by two DACs.

Another common architecture for balanced drivers is the active floating source. This circuit is available in a single-chip, including Analog Devices’ SSM2142 and Texas Instruments’ DRV134/135. Unlike the circuits in Figure 8, the active floating source has very high common-mode output impedances that make the circuit’s stability strongly dependent on cable capacitance and inductance. For this reason, the active floating source is not recommended.

**SUMMARY**

**Do’s**
- Use a balanced line driver to provide good common-mode rejection.
- Use dual op-amps to keep source impedances matched with frequency.
- Minimize output impedance to reduce the dependency of CMRR on impedance mismatches.

**Don’ts**
- Use an active floating source.
5.4 Floating vs. Grounded Voltage Sources

Improperly referenced and/or grounded voltage sources can generate common-mode voltages on the input lines that can exceed the input range of the chip driver’s balanced receivers. Under these conditions, the chip driver will not operate properly. As a general rule, referencing all voltage sources to earth ground will help ensure that the chip driver’s common-mode input range is never exceeded.

All of the chip driver’s internal circuitry is floating with respect to earth ground. In addition, the reference grounds for the two channels are also floating with respect to each other. When a voltage source is connected to one of the inputs, the chip driver’s reference ground for that channel will be connected to the voltage source through a pair of 10 MΩ resistors (see \( Z_{\text{CM1}} \) and \( Z_{\text{CM2}} \) in Figure 7). The chip driver’s reference ground will then float to a voltage equal to any common-mode voltage that is present on the two input lines. Due to this floating, the common-mode voltage “seen” by the chip driver will be close to 0 V, ensuring that the input common-mode voltage range is less likely to be exceeded.

The chip driver’s internal ground can also be referenced through the load, as is the case when the two channels drive intersecting chip traces. The voltage at the point of intersection must be the same for each channel. Due to this constraint, the reference grounds cannot independently float to accommodate common-mode voltages on the two sets of input lines. This can be seen in Figure 9, where a floating voltage source generates a common-mode voltage \( V_{1}^{(cm)} \) on the two input lines of channel 1. A second voltage source, floating with respect to the first, generates a common-mode voltage \( V_{2}^{(cm)} \) on the two input lines of channel 2. Both of these voltages are measured with respect to some common reference \( V_{\text{ref}} \). As shown by the purple line, a current proportional to \( V_{2}^{(cm)} - V_{1}^{(cm)} \) will flow between the two voltage sources.

To minimize common-mode input voltages when driving intersecting chip traces, both voltage sources should be referenced to the same ground \( V_{\text{ref}} \). This is equivalent to setting \( V_{2}^{(cm)} = V_{1}^{(cm)} \). This common ground can also be tied to earth ground, although such a connection is not necessary. If the chip traces do not intersect, then the two channels will be electrically isolated from each other, and they can be driven by voltage sources that are floating with respect to each other.

**SUMMARY**

*Do’s*

- When driving intersecting traces or loads that are electrically connected to each other, reference the control voltage sources to the same ground.
Figure 9: When the chip driver's two channels drive intersecting chip traces, the two voltage sources should be referenced to the same ground. This ensures that common-mode voltages on the two sets of input lines will be the same. If the two voltage sources are floating with respect to each other, different common-mode voltages on the chip driver’s inputs ($V_{1\text{cm}}$ and $V_{2\text{cm}}$, measured with respect to $V_{\text{ref}}$) will induce a current to flow between the sources. In this case, common-mode voltages are more likely to exceed the common-mode input voltage range.
5.5 SHIELDING AND GROUNDING THE INPUT CABLES

This section shows how to connect the chip driver’s inputs to four types of voltage sources:

1. an earth-grounded balanced line driver
2. a floating balanced line driver
3. an earth-grounded single-ended line driver
4. a floating single-ended line driver

These wiring configurations are shown schematically in Figure 10. Earth-grounded balanced line drivers are preferred since they will adhere to the grounding requirements discussed in the previous section for intersecting chip traces (and other loads that are electrically connected). However, if the two channels are driving loads that are not electrically connected, floating line drivers may also be used. In addition, single-ended (i.e. unbalanced) line drivers may be used, although there will be no rejection of common-mode noise and pick-up.

To maximize common-mode rejection of ground noise and electromagnetic interference, the use of shielded, twisted-pair cables is strongly recommended. This section shows where to connect cable shields so that ground loops and shield current induced noise (SCIN) are avoided. In addition, several improper connections involve the cable shields are described.

5.5.1 Proper Wiring of the Control Inputs

The atom chip driver is shipped with two control cables. On one end of each cable, the two signal wires have been soldered to a LEMO plug that mates with the control inputs on the rear panel of the chip driver. The cable drain wires have not been soldered to pin 1 of their respective LEMO plugs. In addition, the cable shield has not been connected to the metal housing of the LEMO plug, as described in Section 5.5.2.3.

The other end of each control cable has not been connectorized. The user should carefully review the following scenarios to determine the proper way to connect the cable's shield and signal wires to voltage sources.

5.5.1.1 Earth-Grounded Balanced Line Drivers (Preferred)

The preferred wiring configuration to the chip driver’s inputs is shown in Figure 10a. Here, a balanced driver that is referenced to earth ground drives a shielded, twisted-pair cable. The cable shield should be directly connected to earth ground only at the voltage source. At the receiver (i.e. the chip driver’s input), the cable shield should not be connected to earth ground or the chip driver’s chassis.

To obtain the best shielding and common-mode rejection, electrical connections from the cable shield to earth ground should be made with wires soldered directly to the ground terminal of the voltage source. Do not rely on the electrical connection to earth ground through a metal enclosure! A soldered wire provides a lower impedance path to earth ground.
5.5.1.2 Floating Balanced Line Drivers

The voltage source may be floating in some situations, such as when the circuit is powered by batteries or a supply that is transformer-isolated from the AC power line (see Figure 10b). In this case, the voltage of the floating reference ground, as measured with respect to the receiver’s ground, will be a common-mode signal that is rejected by the receiver. Ensure that the outputs of the floating source have not drifted out of the receiver’s common-mode input range.

For a floating voltage source, the cable shield should be connected only to the reference ground of the voltage source. At the receiver (i.e. the chip driver’s input), do not connect the cable shield to earth ground or the chip driver’s chassis.

5.5.1.3 Earth-Grounded Single-Ended Line Drivers

The chip driver can be controlled with single-ended voltage sources. However, there will be no rejection of common-mode noise and pickup. To use an earth-grounded single-ended voltage source with a supplied input cable, the LO signal line and the cable shield should be tied together at the output of the voltage source (see Figure 10c). At the receiver (i.e. the chip driver’s input), the shield should not be connected to earth ground or the chip driver’s chassis.

5.5.1.4 Floating Single-Ended Line Drivers

Similar to balanced line drivers, the chip driver may be controlled with a single-ended voltage source that is floating. Again, care must be taken to ensure that the control voltages, as measured with respect to the chip driver’s ground, do not drift out of the chip driver’s common-mode input range. The cable shield should be connected only to the reference ground of the voltage source (see Figure 10d). At the receiver (i.e. the chip driver’s input), the shield should not be connected to earth ground or the chip driver’s chassis.
Figure 10: Connecting the chip driver to a voltage source.  (a) The preferred setup uses an earth-grounded balanced line driver and shielded twisted-pair cable to achieve high rejection of common-noise noise and pick-up.  (b) If the voltage source is floating, the cable shield should be connected to the floating ground of the line driver.  (c) Single-ended voltage sources can be used with the chip driver, although there will be no rejection of common-mode signals.  (d) For a floating single-ended voltage source, the cable shield and negative signal line should both be connected to the floating ground of the voltage source.
5.5.2 Improper Wiring of the Control Inputs

Figure 11 shows three improper techniques for wiring the chip driver’s inputs: a cable shield grounded at both ends, a cable shield connected only at the receiver, and a cable shield connected to the metal housing of the chip driver’s input plug. The problems that arise from these connections are described below.

5.5.2.1 Cable Shield Grounded at Two Points

As indicated by the purple line in Figure 11a, a cable shield grounded at both of its ends creates a ground loop. Due to this loop, voltage noise on the earth ground will drive a noise current through the cable shield. Imperfections in cable manufacturing give rise to imbalances in magnetic and capacitive couplings between the cable’s shield and two signal lines. As a result, currents flowing along the shield will couple differentially into the signal lines. The coupled noise will appear as normal-mode to the receiver, and will therefore not be rejected. This effect is known as shield current induced noise, or SCIN [5].

5.5.2.2 Cable Shield Connected only at Chip Driver

As mentioned in the previous section, imperfections in cable manufacturing give rise to an imbalance in capacitive coupling between the cable’s shield and each of the two signal lines. These cable capacitances interact with the line driver’s common-mode output impedances to form low-pass filters. If the shield is connected only at the chip driver input, as shown in Figure 11b, then voltage noise on the earth ground will be filtered differently on each of the two signal lines. The result is a degradation of common-mode rejection of this ground noise. The problem can be mitigated by always connecting the cable shield at the voltage source and leaving the cable shield unconnected at the chip driver.

5.5.2.3 Cable Shield Connected to Housing of Input Jack

The LEMO plug that connects to the chip driver’s control input has a metal housing that can be internally tied to the cable shield. When this connection is made, the cable shield is directly tied to earth ground through the chip driver’s metal enclosure. This creates the same ground loop shown in Figure 11a. To prevent this ground loop from forming, the cable shield should never be tied to the metal housing of the input plug.
Figure 11: Improper wiring of the atom chip driver's control inputs.
**SUMMARY**

**Do’s**

- Use shielded twisted-pair cable.
- *Always* connect the cable shield directly to reference ground at the signal source. Leave the shield unconnected at the chip driver’s inputs.
- Make connections to earth ground with a star-grounding technique, i.e. solder a wire directly to the earth ground tab on the AC input power module.

**Don’ts**

- Connect the cable shield *only* at the chip driver input.
- Ground the cable shield at both the voltage source and chip driver.
- Connect the cable shield to the metal housing of the input jack.
- Rely on electrical connections to earth ground through a metal enclosure. Instead, use a wire soldered directly to the earth ground tab on the AC input power module.
6. Connecting the Output

The chip driver is shipped with two 6-foot coaxial cables for connecting the outputs to an atom chip. One end of each cable is connectorized to a LEMO plug that mates with the rear-panel output jack (see Figure 5).

6.1 Pin Connections

Figure 12 shows the pin diagram for the output LEMO connectors. A positive current is defined to flow from pin 1 to pin 2. Pin 1 is closest to the red notch.

NEVER connect any of the output connections to earth ground or the chip driver enclosure. The chip driver is designed to have floating outputs, and grounding the outputs will form ground loops that could result in erroneous behavior.

6.2 Output Cable Types

The chip driver is NOT designed to operate with shielded output cables. The use of shielded cables can couple noise onto the outputs.

There are two types of output cables that are recommended for use with the atom chip driver. The first is unshielded twisted-pair. The twisted-pair geometry minimizes coupling of external magnetic fields onto the cables by reducing the area of the magnetic “receiver” formed by the cables, load, and chip driver [2]. Furthermore, since the currents flowing on the two lines are equal and opposite in direction, twisted-pair cables produce a net magnetic field that is zero when averaged over the distance of one twist. Minimizing the magnetic fields generated by the chip currents reduces coupling to other electronics and cables.

The second type of recommended output cable is concentric, or coaxial, cable [2]. Although the outer conductor of this style of cable is usually considered a shield, it does not serve this function in this case. Rather, current returning along the outer conductor produces a magnetic field that cancels the field produced by the current flowing along the center conductor. Similar to the twisted-pair geometry, the area of the magnetic “receiver” is minimized, and coupling of magnetic interference to other electronics and cables is minimized.

6.3 Output Impedance

At frequencies that are low compared to the chip driver’s bandwidth, the output impedance will be very high, approaching the ideal for a true current source. However, at higher frequencies, the device’s open-loop gain drops, causing the chip driver’s output impedance to also drop. In this regime, where the chip driver looks more like a low-impedance voltage source, the actual bandwidth will be determined by filters introduced by the output cables and load. More specifically, the inductance and capacitance of the combined cable and load will act as a low-pass filter. This filter helps reduce output noise at frequencies above the chip driver’s
bandwidth. However, if bandwidth needs to be maximized, use low-inductance cables, keep the lengths of the output cables as short as possible, and reduce the capacitances of the loads.

**SUMMARY**

**Do’s**
- Use twisted-pair or coaxial output cables.
- Use low-inductance cables to improve dynamic performance.

**Don’ts**
- Use shielded output cables.
7. eFuse Protection Circuit

ColdQuanta’s electronic fuse (eFuse) protects against destructive overdriving of the load. The circuit acts like a conventional fuse but is more convenient because its timing characteristics can be adjusted, and it can be easily reset with the simple push of a button. This section describes the operation of the circuit and how to set the circuit’s time constants.

The eFuse generates a signal proportional to the heat generated on the atom chip. The circuit monitors the output current to compute the time-integral of the square of this current. When the value of this integral exceeds the trip setpoint voltage (which is internally set to 1.0 V), a comparator opens up a relay on the output, completely disconnecting the load from all electronics. In addition, the eFuse Open indicator on the front panel will illuminate, notifying the user of an eFuse fault condition. Current cannot flow through the load again until the user manually resets the eFuse by pressing the “On/Off” switch on the front panel.

The output of the time-integrator can be monitored via the eFuse Monitor jack on the front panel. When current flows to the load, the time-integrator voltage increases exponentially until it trips the circuit or reaches a steady-state value. When the output current is reduced – regardless of whether the relay has opened or not – the time-integrator voltage will decrease exponentially back to 0 V.

7.1 TIME CONSTANTS

The eFuse circuit operates with two time constants: one that determines the rate at which the time-integrator voltage exponentially rises (when the chip driver outputs a current), and one at which the same voltage exponentially decays (when the chip driver outputs a reduced current). These time constants are called the charge time constant \( \tau_c \) and the decay time constant \( \tau_d \).

7.2 DETERMINING TRIP TIMES

In order to set the eFuse time constants, the user must provide two pieces of information:

1. The maximum steady-state current \( I_{ss} \) that can flow without tripping the eFuse. For a 100 micron-wide trace on one of ColdQuanta’s GlasSi atom chips, the value \( I_{ss} = 3 \text{ A} \) is recommended. A lower value of this current should be used for narrower traces.

2. The desired trip time \( T_1 \) for a current \( I_1 > I_{ss} \). For the chip driver’s maximum output current of \( I_1 = 5 \text{ A} \), the value \( T_1 = 1 \text{ s} \) is recommended.

The chip driver is shipped with the eFuse time constants set for \( I_{ss} = 3 \text{ A} \) and \( T_1 = 1 \text{ s} \) at \( I_1 = 5 \text{ A} \).
The time constants $\tau_c$ and $\tau_d$ are set by two resistances, labeled here as $R_c$ and $R_d$. The steady-state current $I_{ss}$ determines the ratio of $R_c$ and $R_d$ according to the relation

$$\frac{R_d + 10^4 \Omega}{R_c + 10^4 \Omega} = \frac{1}{I_{ss}^2}.$$

All values are expressed in SI units. A resistance of $10^4 \Omega$ is connected in series with $R_d$ and $R_c$, each of which can be adjusted between 0 and 1 MΩ. The trip time $T_1$ and trip current $I_1$ then determine the charge time constant according to the relation

$$\tau_c = \frac{T_1}{\log \left[1 - \left(\frac{I_{ss}}{I_1}\right)^2\right]}.$$

The value of $R_c$ is then given by

$$R_c = \tau_c \times 10^5,$$

while the decay time constant is given by

$$\tau_d = \left(R_d + 10^4 \Omega\right) \times 10^{-5} = \frac{\left(R_c + 10^4 \Omega\right)}{I_{ss}^2} \times 10^{-4}.$$

When the circuit is excited by a step-function of height $I$ applied at $t = 0$, the time-integral voltage will be

$$V(t,I) = (1 - e^{-t/\tau_c}) \times \left(\frac{I}{I_{ss}}\right)^2.$$

This voltage will appear on the eFuse monitor jack. The trip time $T_{tr}$ as a function of applied current $I$ is given by

$$T_{tr}(I) = -\tau_c \times \log \left[1 - \left(\frac{I_{ss}}{I}\right)^2\right], \text{ for } I > I_{ss}.$$

An important note about the decay time constant: the monitor voltage decays exponentially because the time-integrator is “leaky.” This leaky integrator models how heat produced by the atom chip dissipates into the surrounding environment. Immediately resetting the eFuse after it trips can cause it to quickly trip again if the time-integrator has not had a chance to decay much below 1 V. Therefore, the user may have to wait several seconds before resetting the eFuse and proceeding. This delay is intentional, as it gives the atom chip a chance to cool off.
CAUTION!

To reduce the likelihood of burning out the atom chip, ERR ON THE SIDE OF CAUTION when choosing values for the eFuse time constants. In addition, take into consideration intersecting chip traces. The currents flowing down the two traces will pass through the conductor where the traces overlap. Since power dissipation scales as the square of the total current, power dissipation in this region will be greater than that from the two currents when considered individually. This extra heat makes intersections likely places for burn-outs to occur.
7.3 Setting the Charge and Decay Times

Once values for $I_{SS}$ and $T_1$ have been chosen, the user can set $R_c$ and $R_d$ with a pair of 1 MΩ trimpots that are located on the top edge of the current source boards inside of the chip driver. Turning the trimpot actuators clockwise increases the resistance.

**HIGH VOLTAGE WARNING!**

Setting the eFuse time constants requires operating the chip driver with its top panel removed. *High voltages from the AC power line will be present!* Use adequate safety precautions to prevent the risk of electric shock.

**CAUTION!**

Do *NOT* connect an atom chip to the chip driver output when setting the charge and decay time constants! This presents an unnecessary risk to the atom chip. Instead, short the chip driver’s output. The eFuse settings are independent of the load.

Figure 13: The eFuse time constants can be set with the internal trimpots labeled in this top-down view. The front panel of the atom chip driver is located to the left of the image, while the rear panel is located to the right.
Use the following procedure to set the eFuse time constants:

1. Remove the top panel of the chip driver’s enclosure.

2. Adjust $R_d$ (decay time constant trimpot) fully clockwise and $R_c$ (charge time constant trimpot) fully counterclockwise.

3. Attach the eFuse monitor to an oscilloscope, and set the time scale to a large enough value so that you can see several seconds of response. Wait for the eFuse monitor voltage to decay to 0 V, if it’s not already there.

4. Short the chip driver output (do not run this test on a real atom chip!). The trip times are independent of load.

5. Apply the appropriate voltage to the chip driver input to set the output current to $I_1$ (e.g. for $I_1 = 5.0$ A, set the input voltage to 5.0 V).

6. Press the “Output On/Off” button to enable the chip driver’s output. On the oscilloscope, measure the time it takes for the eFuse voltage to reach the trip point of 1.0 V. This time should equal $T_1$. If this time is greater than $T_1$ or the voltage reaches a steady-state value below 1.0 V, adjust $R_c$ clockwise a half-turn. If the time is less than $T_1$, adjust $R_c$ counterclockwise a half-turn. If the eFuse has not tripped, press the “Output On/Off” button to disable the output. Go to Step 6.

7. Apply the appropriate voltage to the chip driver input to set the output current to $I_{ss}$ (e.g. for $I_{ss} = 3.0$ A, set the input voltage to 3.0 V).

8. Turn the output current on by pressing the “Output On/Off” button.

9. Adjust $R_d$ counterclockwise until the eFuse voltage on the oscilloscope is just under 1.0V. Be sure to wait until the eFuse voltage reaches steady state. If the eFuse voltage exceeds 1.0 V and the eFuse trips, adjust $R_d$ a half-turn clockwise. Enable the output by pressing the “Output On/Off” button and verify the eFuse voltage is just below 1.0 V. Once the steady-state eFuse voltage is just below 1.0 V, press the “Output On/Off” button to disable the output and go to Step 9.

10. The process is iterative, so if $R_c$ was adjusted in step 8, then go back and repeat steps 4 through 8 until the desired maximum steady-state current is $I_{ss}$, and the current $I_1$ trips the circuit in time $T_1$. Usually two or three iterations are needed to achieve a timing accuracy of 1%.
7.4 CROSSED-CHANNEL OPERATION

As an extra level of protection, the eFuse circuits in the atom chip driver can be operated in a crossed-channel configuration. More specifically, channel 1’s eFuse will respond not only to channel 1’s output, but to channel 2’s output as well. This is achieved by summing the two channels’ time-integrator voltages before comparing to the trip setpoint voltage. With this approach, each eFuse responds to the sum of the powers dissipated by both channels.

One consequence of crossed-channel eFuse operation is that both eFuse circuits will trip simultaneously. This behavior is intentional, as it errs on the side of protection. When both eFuse circuits trip, both channels’ outputs will need to be manually reset by pressing both “Output On/Off” buttons on the front panel.

To remove crossed-channel operation, disconnect at least one of the two jumper cables labeled in Figure 14. This procedure requires removing the top panel of the chip driver’s enclosure. With crossed-channel operation disabled, each channel’s eFuse circuit will continue to operate, but only for that channel’s output.

![Figure 14](image)

Figure 14: Crossed-channel operation of the eFuse circuitry can be disabled by removing one of the two internal jumper cables indicated by the yellow arrows.
## 8. Troubleshooting

<table>
<thead>
<tr>
<th>Description</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>“Main Power” indicator does not illuminate when button is depressed.</td>
<td>The unit is not receiving power from the input AC (mains) line:</td>
</tr>
<tr>
<td></td>
<td>• Ensure that the power cord is properly inserted into a three-prong protective-grounded power output.</td>
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<tr>
<td></td>
<td>• Ensure the power cord is properly plugged into the input power module on the back of the chip driver.</td>
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<td></td>
<td>• Check that the correct fuse has been inserted into the fuse holder on the back of the chip driver. If the fuse is blown, replace</td>
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<td>with a fuse of the same current rating, voltage rating, and type (i.e. slo-blo, fast blo, etc.).</td>
</tr>
<tr>
<td>“Output On/Off” indicator does not illuminate when button is depressed.</td>
<td>• Ensure that the unit is properly powered from the AC (mains) line.</td>
</tr>
<tr>
<td></td>
<td>• If the unit is properly powered from the AC (mains) line, a fault condition may be immediately causing the unit to disable its output.</td>
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<tr>
<td></td>
<td>Check if one of the fault LED indicators on the front panel is illuminated. If so, refer to the description below associated with</td>
</tr>
<tr>
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<td>that fault.</td>
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<tr>
<td>No current is outputted when the “Output On/Off” indicator is illuminated.</td>
<td>• Check that the input control lines are properly connected to both the voltage source(s) and the chip driver’s input jacks on the</td>
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<td></td>
<td>rear panel.</td>
</tr>
<tr>
<td>Output current does not reach the maximum specification of ±5 A.</td>
<td>• Check that the load resistance $R_{LOAD}$ is less than 1 Ω.</td>
</tr>
<tr>
<td></td>
<td>• If $0.5 , \Omega &lt; R_{LOAD} &lt; 1 , \Omega$, the maximum output current specification is ±3 A.</td>
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<td></td>
<td>• When the chip driver is driven with floating voltage sources, the reference ground may have exceeded the common-mode input voltage</td>
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<td>range of the chip driver. Switch to earth-grounding of the voltage sources.</td>
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<tr>
<td>“Overtemp” LED indicator is illuminated.</td>
<td>• The internal circuitry of the chip driver is too hot. Wait several minutes for the circuits to cool down. If this problem occurs</td>
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<td>repeatedly, move the unit to an area where there is better air flow.</td>
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<tr>
<td>“Open Circuit” LED indicator is illuminated.</td>
<td>• The chip driver does not see a load. Ensure that the output cable is properly connected to the atom chip.</td>
</tr>
<tr>
<td></td>
<td>• If the output is properly connected, ensure that the total load resistance $R_{LOAD}$ is less than 1 Ω.</td>
</tr>
<tr>
<td></td>
<td>• If $0.5 , \Omega &lt; R_{LOAD} &lt; 1 , \Omega$, the chip driver’s maximum output current is only guaranteed to ±3 A. Ensure that the</td>
</tr>
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<td></td>
<td>differential input voltage does not exceed ±3 V.</td>
</tr>
<tr>
<td>“eFuse Open” LED indicator is illuminated.</td>
<td>• The eFuse circuit has tripped. Reset the circuit by pressing the “Output On/Off” button. If the circuit is tripping repeatedly,</td>
</tr>
<tr>
<td></td>
<td>consider increasing the charge and/or decay time constants.</td>
</tr>
</tbody>
</table>
9. References


10. Limited Warranty

1. Definitions
   a) “Delivery” means standard ColdQuanta shipping to and arrival at the receiving area at the “Ship To” address specified in Customer’s Order.
   b) “Exhibits” means attachments that describe or otherwise apply to the sale of Products.
   c) “Products” means hardware, documentation, accessories, supplies, parts and upgrades that are determined by ColdQuanta to be available from ColdQuanta upon receipt of Customer’s Order. “Custom Products” means Products modified, designed or manufactured to meet Customer requirements.
   d) “Specifications” means specific technical information about ColdQuanta Products that has been delivered by ColdQuanta to the Customer with Customer’s Order.
   e) “Support” means hardware maintenance and repair; training; and other standard support services provided by ColdQuanta. “Custom Support” means any agreed nonstandard support, including consulting and custom project services.

2. Limited Warranty
   a) ColdQuanta warrants ColdQuanta hardware Products against defects in materials and workmanship for a period of one year from the delivery date.
   b) ColdQuanta does not warrant that the operation of Products will be uninterrupted or error free.
   c) If ColdQuanta receives notice of defects, ColdQuanta will, at its option, repair or replace the affected Products. If ColdQuanta is unable, within a reasonable time, to repair, replace or correct a defect or non-conformance in a Product to a condition as warranted, Customer will be entitled to a prorated refund of the purchase price upon prompt return of the Product to ColdQuanta. Such refunded amount will be prorated based on a four-year straight line depreciation schedule. Customer will pay expenses for return of such Products to ColdQuanta. ColdQuanta will pay expenses for shipment of repaired or replacement Products.
   d) ColdQuanta warrants that ColdQuanta Support will be provided in a professional and workmanlike manner. Some newly manufactured ColdQuanta Products may contain and ColdQuanta Support may use remanufactured parts that are equivalent to new in performance.
   e) The above warranties do not apply to defects resulting from:
      (i) improper or inadequate maintenance by Customer;
      (ii) customer or third party supplies;
      (iii) unauthorized modification;
      (iv) improper use or operation outside of the Specifications for the Product;
      (v) abuse, negligence, accident, loss or damage in transit;
      (vi) improper site preparation; or
      (vii) unauthorized maintenance or repair.
   f) THE ABOVE WARRANTIES ARE EXCLUSIVE AND NO OTHER WARRANTY, WHETHER WRITTEN OR ORAL, IS EXPRESSED OR IMPLIED. TO THE EXTENT PERMITTED BY LAW, COLDQUANTA SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT.